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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,888	11/21/2003	Akiyoshi Aoyagi	81754.0101	1432

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/719,888	AOYAGI, AKIYOSHI	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *6 and 7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Japanese patent application No. 2002-340879 filed on November 25, 2002 which papers have been placed of record in the file.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled .on November 21, 2003

The references on PTO 1499 submitted on 11/21/2003 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Election/Restrictions

Applicant's election without traverse of group I claims 1-5 and 8-20 in the reply filed on November 22, 2004 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 lines 1-2 recite "an electronic device comprising a semiconductor device recited in any one of claim 1. "

It is not clear if Applicants' intend claim 8 to depend upon claim 1 only or claim 1 and any other claim , thus impossible to determine the exact scope of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 , 8-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipate by Akram et al. (U.S. Patent No. 5,994,166, herein after Akram) .

With respect to claim 1 Akram describes a semiconductor device, comprising: a base substrate including a base wiring pattern; (Akram figure 1 # 102, col. 5 line 57) a first circuit substrate disposed over the base substrate and including a first wiring pattern; a first semiconductor element mounted on the first circuit substrate (Akram fig. 1# 116, col. 6 lines 1-2) and including a first electrode electrically connected to the first wiring pattern; (Akram figure 4 # 418, col. 7 lines 45-49) a second circuit substrate

disposed over the first circuit substrate (Akram figure 4 # 440 , col.8 line 2) and including a second wiring pattern; (Akram figure 4 # 460) a second semiconductor element mounted on the second circuit substrate (Akram figure 4 # 452, col.8 line 14) and including a second electrode electrically connected to the second wiring pattern; (Akram figure 4 # 460, col. 8 lines 19-20) a first protruded electrode electrically connected to the first wiring pattern and protruding from the first circuit substrate and bonded to the base wiring pattern; (Akram figure 6 # 716, col. 9 line 65 to col. 10 line 5 similar to 22 described in Applicants specification page 6-8) and a second protruded electrode electrically connected to the second wiring pattern and provided protruding from the second circuit substrate and bonded to the base wiring pattern. (Akram figure 6 # 724, col.9 line 65 to col. 10 line 5 similar to 22 described in Applicants specification page 6-8).

With respect to claim 2 Akram describes the semiconductor device according to claim 1, further comprising a third semiconductor element mounted on the base substrate and including a third electrode electrically connected to the base wiring pattern. (Akram figure 4 # 462, col. 8 lines 21-25) .

With respect to claim 3 Akram describes the semiconductor device according to claim 1, wherein the second protruded electrode is thicker than the first protruded electrode. (Akram figure 6 # 726, similar to Applicants' figure 3 # 23 and 32) .

With respect to claim 4 Akram describes the semiconductor device according to claim 1, further comprising another semiconductor element layered on the first

semiconductor element. (Akram figures and col. 9 lines 40-45, plurality of semiconductor devices) .

With respect to claim 5 Akram describes the semiconductor device according to claim 1, further comprising another semiconductor element layered on the second semiconductor element. (Akrtam figures and col. 9 lines 60-63).

With respect to claim 8 , to the extent understood, Akram describes an electronic device comprising a semiconductor device recited in any one of claim 1. (rejected for same reasons as set out in claim 1).

With respect to claim 9 Akram describes the semiconductor device according to claim 1, wherein the base substrate is equipped with a dielectric substrate material. (Akram figure 1 # 416, col. 7 lines 44-45).

With respect to claim 10 Akram describes the semiconductor device according to claim 1, wherein the base wiring pattern has a multiple layered wiring structure. (Akram col. 9 lines47-50, not shown in drawings).

With respect to claim 11 describes the semiconductor device according to claim 1, wherein the second semiconductor element includes electrodes. (Akram col. 10 lines 35-36, 43 etc. memory chips CPU –all devices having electrodes) .

With respect to claim 12 Akram describes the semiconductor device according to claim 1, wherein the base wiring pattern includes lands bonded to the first and second protruded electrodes. (Akram col. 4 lines 40 to 50, 60-65, figure 4,etc.) .

With respect to claim 13 Akram describes the semiconductor device according to claim 1, wherein the first and second protruded electrodes are bonded to the base

wiring pattern selected from the group consisting of anisotropic conductive adhesive, dielectric adhesive, alloy bonding, metal bonding and inter-metal diffusion bonding.Akram col. 4 lines 5-15, col. 3 line 10, etc.).

With respect to claim 14 Akram describes the semiconductor device according to claim 11, wherein the electrodes are formed from electrode pads. (col. 4 lines 15-16, 37-44, etc.)

With respect to claim 15 Akram describes the semiconductor device according to claim 11, wherein the electrodes of the second semiconductor element are electrically connected to the second wiring pattern by a face-down bonding method. (Akram Abstract –line2, col. 1 line24, etc.) .

With respect to claim 16 Akram describes the semiconductor device according to claim 11, wherein the electrodes of the second semiconductor element are electrically connected to the second wiring pattern by a wire-binding method. (sic- wire bonding, col. 1 lines 63 to col. 2 line13)

With respect to claim 17 Akram describes the semiconductor device according to claim 1, wherein the protruded electrodes are formed from a conductive member. (inherent- electrodes have to conduct electricity and must be formed of conductive material)

With respect to claim 19 Akram describes the semiconductor device according to claim 17, wherein the conductive member is selected from the group consisting of a metal, a metal compound, an alloy, a conductive paste and a solder metal. (Akram , col. 10 lines 2-4, 13-15, etc.) .

With respect to claim 20 Akram describes a semiconductor device, comprising a base substrate including a base wiring pattern (Akram figure 1 #102, col. 5 line 57) a first circuit substrate disposed over the base substrate (Akram fig. 1 #166, col. 6 lines 1-2)and including a first wiring pattern (Akram col. 7 lines 45-49) a first semiconductor element mounted on the first circuit substrate and including a first electrode electrically connected to the first wiring pattern; (Akram figure 4 #452, col. 8 line 14) a second circuit substrate disposed over the first circuit substrate and including a second wiring pattern; a second semiconductor element mounted on the second circuit substrate and including a second electrode electrically connected to the second wiring pattern; (Akram figure 6 # 724, col. 9 line 65 to col. 10 line 5) and means for electrically connecting to the first and second wiring patterns, protruding from the first and second circuit substrates and bonding to the base wiring pattern. (Akram figure 4) .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (U.S. Patent No. 5,994,166, herein after Akram) as applied to claims 1-5, nad 8-

17 above and further in view of Imasu et al. (U.S. Patent NO. 6,737,741, herein after Imasu).

With respect to claim 18 Akram describes the semiconductor device according to claim 17, wherein the conductive member includes a structure in which a plurality of conductive films are stacked in layers.

Akram does not specifically describe the conductive member includes a structure in which a plurality of conductive films are stacked in layers.

However , Yoneda et al. a patent from the same filed of endeavor describes in the brief summary section a plurality of stacked metal electrodes to provide better chip density, good current density, higher purity and ease of performing subsequent method steps without problems of destroying the structure formed.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yoneda's conductive member includes a structure in which a plurality of conductive films are stacked in layers in Akram's device to provide better chip density, good current density, higher purity and ease of performing subsequent method steps without problems of destroying the structure formed.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718 . The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Steven H. Rao

Patent Examiner

Feb 04 05

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